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EXAMINER	
HASSAN, AURANGZEB	

ART UNIT	PAPER NUMBER
2182	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,996	HOMEWOOD ET AL.	
	Examiner	Art Unit	
	AURANGZEB HASSAN	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 March 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3 – 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis et al (U.S. Patent No. 5,797,043 hereinafter "Lewis") in view of George et al. (US Patent Number 6,785,829, hereinafter "George") further in view of Horning (US Patent Number 5,420,998).

3. As to Claims 1 and 24, Lewis teaches a system comprising:

a processor comprising an execution for executing instructions; (Host Processor, element 12, figure 1a)

a stream register unit configured to supply a first type of data to the execution unit, the first type of data being data supplied from a peripheral (I/O Channel Controller, element 62, figure 3, element 140, figure 5a), the stream register unit including at least one stream register unit FIFO configured to store the first type of data received from the peripheral (FIFO pool 172, figure 5a);

a FIFO coupled to the peripheral to receive said first type of data from the peripheral (column 14, lines 25 – 29) and connected to the stream register unit by a

communication path (FIFO Pool Bus 144, figures 5a and 6), along which said first type of data can be supplied from the FIFO to the at least one stream register unit FIFO (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6); and

a memory bus, separate from the communication path, connected between a data memory and the processor, across which the processor can access the second type of data, the second type of data being randomly accessible data held in the data memory (Processor Bus, element 16', figure 2);

wherein the first type of data is supplied via the communication path directly from the FIFO coupled to the peripheral to the stream register unit of the processor (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6) and the second type of data is supplied via the memory bus, separate from the communication path, between the data memory and the processor (Processor Bus, element 16', figure 2)

wherein the stream register unit is configured to:

in response to a request for a data item from the execution unit, when the data item is located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit (FIFO pool subsystem, figure 6, FIFO memory is connected via FIFO pool bus 144 as can be seen in figures 5a and 6).

Lewis fails to teach a system wherein a stream register unit being part of the processor.

George teaches, in an analogous system, a system wherein the stream register unit (cache, element 365, figure 3) forms part of the processor (processor, element 300, figure 3).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of George. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to efficiently optimize a system with regards to real estate in compactness and means of high-speed processing.

The combination of Lewis and George fails to teach system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions.

Horning teaches a system, wherein a processing unit is configured to, when the processing unit does not contain the data item in the next location, request the data item from the memory coupled to the peripheral, and send a stall signal to the execution unit, causing the execution unit to stop executing instructions (column 11, lines 5 – 15, when the predetermined level is at empty is considered the point at which the next data item is not available and the system issues a request from the source which is analogous to the peripheral and halts the data transfer which is considered the stall signal which stops the execution of the transfer instruction).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above

teachings of Horning. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system (column 5, lines 11 – 18).

4. As to claim 3, Lewis teaches a system, wherein data is supplied from the FIFO to the stream register unit accordance with requests for data made (requested function, column 13, 23 – 30) by the processor to the stream register unit and forwarded to the FIFO (FIFO pool buffering functions, column 12, lines 38 –58).

5. As to claim 4, Lewis teaches a system, wherein the said requests are made as accesses to volatile variables (10 Bit – Request variable changes consistently per requested lines of data and can be changed at any time, Table VIII).

6. As to claim 5, Lewis teaches a system wherein the FIFO is arranged to, upon receiving a request for data from the stream register unit, send a signal to the stream register unit indication availability of the requested data (available space and data, Table VII sent via BTU, element 170 figure 5b.).

7. As to claim 6, Lewis teaches a system, wherein if the FIFO contains the requested data, the said signal to the stream register unit indicates that the data is available, and the FIFO is further arranged to send (burst data transfer, column 20, lines

1 – 4) a signal (transfer signals, Table VI) to the stream register unit comprising the data (column 19, lines 64 – 67, column 20, lines 1 – 35).

8. As to claim 7, Lewis teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, supply the data (data stream, element 76, figure 3) to the execution unit (column 10, lines 25 – 41, passed to DSP, column 20 lines 5 - 35).

9. As to claim 8, Lewis teaches a system, wherein the stream register unit is arranged to, following receipt of the signal comprising the data, send a signal to the FIFO indicating that it has taken the data (Transfer Done, Table VII).

10. As to claim 9, Lewis teaches a system, wherein the said signal to the FIFO further indicates the next location in the FIFO from which the data is required (next sequential, column 16, lines 10 – 33).

11. As to claim 10, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

The combination of Lewis and George fails to teach system wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available.

Horning teaches a system, wherein the FIFO is further arranged to, if it does not contain the requested data, send a different signal to the stream register unit indicating that the data is not available (column 11, lines 5 – 15, when the predetermined level is at empty is considered the point at which the data item is not available and the system issues the stall signal which stops the execution of the transfer instruction).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above teachings of Horning. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system (column 5, lines 11 – 18).

12. As to claim 11, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

The combination of Lewis and George fails to teach system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions.

Horning teaches a system, wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the execution unit, causing the processor to stop executing instructions (column 11, lines 5 – 15, when the predetermined level is at

empty is considered the point at which the data item is not available and the system issues the stall signal which stops the execution of the transfer instruction).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above teachings of Horning. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system (column 5, lines 11 – 18).

13. As to claim 12, Lewis teaches a system comprising a FIFO connected to receive data from the peripheral and connected to the stream register unit.

The combination of Lewis and George fails to teach system wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit.

Horning teaches a system, wherein the FIFO is further arranged to, if following sending of the said different signal to the stream register unit indicating that the data is available and to send a signal comprising the data to the stream register unit (column 11, lines 5 – 25, when the predetermined level is at empty is considered the point at which the data item is not available and the system issues the stall signal which stops the execution of the transfer instruction).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Lewis and George with the above

teachings of Horning. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to handle multiple delayed transactions in a system (column 5, lines 11 – 18).

14. As to claims 13 and 25, Lewis teaches a system, further comprising a timeout generator, arranged for communication with the processor and the stream register unit, and arranged to, if the signal sent by the FIFO is a signal indicating that the data is not available (data available in the FIFO, Table VIII), after a predetermined period of time, send a timeout signal to the execution unit, causing the processor to interrupt (Interrupt, Table III & XXIV) such that it can execute other instructions (column 36, lines 1 – 17).

15. As to claim 14, Lewis teaches a system, wherein if following sending of the timeout signal to the execution unit the data subsequently becomes available, the timeout generator is arranged to receive a signal instructing it to cease sending the timeout signal, and to, upon receipt of the said instruction, cease sending the timeout signal (column 36, lines 18 – 40).

16. As to claim 15, Lewis teaches a system, wherein the stream register unit is arranged to, if following sending of the timeout signal to the execution unit the data subsequently becomes available, send the data to the execution unit (in response to host interrupts, the host processor provides for the transfer of data, column 26, lines 25 – 34).

17. As to claim 16, Lewis teaches a system, wherein the stream register unit is associated with a register file containing a plurality of registers (register based interface, column 22, lines 15 – 33) and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 19, lines 52 – 63).

18. As to claim 17, Lewis teaches a system, wherein the execution unit is arranged to retrieve data from the register file (column 22, lines 15 – 33).

19. As to claim 18, Lewis teaches a system, wherein data is supplied from the FIFO to the stream register unit in accordance with requests for data made by the processor to the stream register unit and forwarded to the FIFO (figure 1a and 1b), wherein the stream register unit is associated with a register file containing a plurality of registers and a load/store unit arranged to receive data from the stream register unit and temporarily store the data in the register file (column 19, lines 52 – 63), wherein the execution unit is further arranged to make requests for data to the stream register unit via the load/store unit (column 33, lines 33 – 39).

20. As to claim 19, Lewis teaches a system, wherein the stream register unit comprises one or more FIFOs connected to receive data from the FIFO connected to the stream register unit and supply the data to the execution unit (FIFO 0 – 3, elements 210 – 212, figure 5c).

21. As to claim 20, Lewis teaches a system, wherein the request for data is a request for a single data item (column 10, lines 30 - 41).

22. As to claim 21, Lewis teaches a system, further comprising one or more additional FIFOs linked (FIFO 0 – 3, elements 210 – 212, figure 5c) together between the said FIFO and the communication channel (FIFO pool subsystem, figure 6).

23. As to claim 22, Lewis teaches a system, wherein the data from the peripheral is video data (video words, column 25, lines 37 – 40).

24. As to claim 23, Lewis teaches a system, wherein the peripheral is a video processing system (video controller, column 25, lines 29 – 48).

25. Claim 26 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lewis in view of Garcia et al. (US Patent Number 6,433,785 hereinafter "Garcia").

26. As per claims 26 and 30, Lewis teaches a stream register being part of a processor comprising an execution unit, the stream register being connectable between the execution unit and peripheral and between the execution unit and a memory, comprising:

a receiver arranged to receive a request for a data item from the execution unit (column 10, lines 30 - 41); at least one FIFO configured to store the data item received form the peripheral (FIFO pool 172, figure 5a); and

a stream engine (element 76, figure 3), arranged to send the request to the peripheral and receive one or more signals back from the peripheral indicating availability of the requested data item (I/O Channel Controller, element 62, figure 3), and, when the data item is available (available space and data, Table VII sent via BTU, element 170 figure 5b.), send the data item to the execution unit of the processor.

Lewis fails to teach a register wherein when the data item being requested is not available, sending a timeout signal to the processor.

Garcia teaches a register wherein when the data item being requested is not available, sending a timeout signal to the execution unit of the processor (timeout counter, column 5, lines 26 – 42)

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Lewis with the above teachings of Garcia. One of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modifications in order to optimize a request process in which resources are valuable and delays need to be minimized, improving processor to device throughput.

27. As to claim 27, Lewis teaches a stream register, wherein the stream engine is arranged to send the timeout signal to the execution unit of the processor after a predetermined period of time (Interrupt, table III).

28. As to claim 28, Lewis teaches a stream register, wherein the stream engine is further arranged to, when the data is available, temporarily store the data in a register file for access by the execution unit of the processor (temporarily stored in a FIFO within the bus master units, column 19, lines 52 – 63).

29. Lewis modified by the teachings of Garcia as applied to claims 26 and 30 above, in regards to claim 29, Lewis teaches a stream register, wherein the stream engine is further arranged to temporarily store (column 19, lines 52 – 63) the data in a register file for access by the execution unit (column 18, lines 29 – 36).

Lewis fails to teach a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the execution unit of the processor, when the data item subsequently becomes available, receive a signal instructing it to cease sending the timeout signal, and to upon receipt of the said instruction cease sending the timeout signal to the processor.

Garcia teaches a stream register, wherein the stream engine is further arranged to, following sending of the timeout signal to the processor, when the data item subsequently becomes available (posted write buffer available signal 350, column 5, lines 30 – 31), receive a signal instructing it to cease sending the timeout signal, and to

upon receipt of the said instruction cease sending the timeout signal to the processor (column 5, lines 26 – 42).

Response to Arguments

30. Applicant's arguments filed 3/13/2009 have been fully considered but they are not persuasive. The Applicant argues that Lai does not teach a stall signal that stops a transaction when data is not available. The structure of claims 26 and 30 are not recited in the prior art and lastly that the timeout signal of Garcia is not the same as the claimed invention.

The Examiner notes that in order to overcome the rejection as cited the Applicant should reflect the claim language to depict the differences in the claimed structure of the FIFO/processor/register to peripheral system as best depicted in figure 4.

In response to applicant's argument regarding Lai, the Examiner has cited Horning for the teachings of sending a stop signal to stop execution of instructions if the next data item is not available and further issuing a request for the next data item from the source peripheral.

In response to applicant's arguments, the recitation of the structural differences of the processor of claims 26 and 30 has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand

alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

With regards to Garcia not teaching a timeout signal the Examiner respectfully disagrees. The applicant has elaborated on alternate embodiments of Garcia to show that the timeout signal may vary from that of instant application how explicitly pointing out differences in the specification without have such characteristics necessitated by the claims does not overcome the rejection. The claims necessitate a timeout signal that allows other applications to execute. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to AURANGZEB HASSAN whose telephone number is (571)272-8625. The examiner can normally be reached on Monday - Friday 9 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571)272-6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AH

/Tariq Hafiz/
Supervisory Patent Examiner, Art Unit 2182